

REMARKS

Status of the Application

Claims 1-4 are the claims that have been examined in the present application. Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schmoock et al., (U.S. Patent No. 6,624,994) in view of Andruzzi et al. (U.S. Patent No. 6,377,032).

Preliminary Matters

Applicant thanks the Examiner for withdrawing the §103(a) rejection of claims 1-4 over Schmoock in view of Taki (U.S. 6,474,762).

Further, Applicant thanks the Examiner for withdrawing the objections to claim 1 and 3 as lacking antecedent basis.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Schmoock et al., (U.S. Patent No. 6,624,994) in view of Andruzzi et al. (U.S. Patent No. 6,377,032).

The Examiner alleges that a combination of Schmoock and Andruzzi would render claims 1-4 obvious. The Examiner uses a similar argument as presented in the Office Action dated October 19, 2005, with the exception that the Examiner alleges that Andruzzi, instead of Taki, discloses “setting a constant of the circuit element so that the reference voltage is not greater than a critical voltage, wherein the critical voltage is a product of an on-resistance of the semiconductor device when its channel temperature is at an upper limit of a permissible temperature, and a minimum current value which causes the channel temperature to reach the upper limit of the permissible temperature by the self-heating due to Joule heat.”

Applicant respectfully submits that claims 1-4 are patentable over Schmoock in view of Andruzzi because (i) Andruzzi fails to teach setting a constant of the circuit element so that the reference voltage is not greater than a critical voltage, as recited in claim 1, and thus fails to cure the defects of Schmoock conceded by the Examiner, and (ii) the Examiner has failed to provide any objective evidence that it would have been obvious to combine Schmoock and Andruzzi.

(i) The Examiner cites col. 3, lines 12-21 and 23-26 of Andruzzi as teaching setting a constant of the circuit element so that the reference voltage is not greater than a critical voltage. The Examiner alleges that the cited portion of “Andruzzi teaches that it is well known in the art to use a product of the current and voltage through and across the switch to set a threshold or critical voltage, and it is well known for the voltage to be selected based on current flow that would cause overheating when the circuit operates in its expected environment.” See Office Action, page 3. Applicant respectfully submits that the Examiner is misreading the teaching of Andruzzi.

The description disclosed in col. 3, lines 12-26 of Andruzzi discloses three things: 1) a current flowing in FET can be measured by using V_{DS} (voltage applying between a drain and a source) of FET; 2) V_{ps} is changed, while I_{DS} is constant, when $R_{DS(ON)}$ is changed; and 3) the measurement accuracy as the current sensor is low since $R_{DS(ON)}$ is considerably changed on the basis of the change of the temperature. Therefore, the cited description of Andruzzi does not teach or suggest a method of setting a determinant value for the excess current. Further, Andruzzi fails to teach or suggest that a constant of the circuit element should be set so that the reference voltage is not greater than a critical voltage. Andruzzi simply notes that a relationship exists between resistance, current, and temperature. Nowhere does Andruzzi disclose that a

circuit element should be set so that a reference voltage is not greater than a critical voltage based on the on-resistance at an upper limit of a permissible temperature and a minimum current value causing the temperature to reach the upper limit of the permissible temperature. Therefore, Andruzzi fails to cure the defects of Schmoock conceded by the Examiner.

(ii) The Examiner has failed to provide any objective evidence regarding a motivation to combine Schmoock and Andruzzi. The burden is on the Examiner to demonstrate using only objective evidence or suggestion from the applied prior art, that one of ordinary skill would have been lead to the claimed invention as a whole without recourse to Appellant's disclosure. See: In re Oetiker, 977 F.2d 1443, 1447-48, (Fed. Cir. 1992); In re Fine 837 F.2d 1071, 1074-75, (Fed. Cir. 1988) (emphasis added). As a matter of law then, it is the burden of the Examiner to demonstrate that the prior art, and not Appellant's disclosure, would lead the hypothetical artisan to the claimed invention as a whole.

In the present Office Action, the Examiner fails to cite any portion of Scmoock or Andruzzi in which there is a teaching or suggestion that the references may be combined as alleged by the Examiner. The fact that each individual reference provides protection of a semiconductor device is insufficient to show that the references are combinable. Therefore, because the Examiner has failed to provide any objective evidence that the references may be combined, the Examiner has not met the burden required in establishing a *prima facie* case of obviousness with regard to claim 1.

For the reasons noted above, claim 1, and by analogy, claim 3 should be patentable over the applied art. Claims 2 and 4 should be patentable over the applied art at least by virtue of their dependency from claims 1 and 3, respectively.

Response under 37 C.F.R. § 1.111
U.S. Application No. 10/519,745

Attorney Docket No. Q85443

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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